REMARKS

Reconsideration of the application, in view of the following amendments and remarks is respectfully requested.

The Examiner objects to Claim 1 because on line 11 “to the sent” should be -- to be sent--. The claim has been so corrected. The Examiner asked how the empty flags are generated. As recited in the claims and as discussed in the specification in the paragraph 0005, the empty flags are generated by the queue. This is clearly shown in Figure 1 of the present application.

The Examiner objects to drawings under 37 C.F.R. 1.83(a) that the drawings must show every feature of the invention specified in the claims. The Examiner states that therefore the arbitrator comprised in the data queues, the arbitration table with its multiple entries and the arbitrator logic circuit must be shown or the features cancelled from the claims. The Examiner states that in addition, the first multiplexer should be shown operatively receiving an output from a first table entry and an output from the second table entry in the arbitration table.

Applicants believe that the drawings presently on file clearly illustrates the features specified in the claims. Furthermore, Applicants have amended the claims to a “in a weighted round-robin arbitrator comprising” format which should obviate the Examiner’s objection. In the present invention, the look-up table 120 shown in Figure 1 is replaced with the table 202 shown in Figure 2. See, for example, the first four lines of paragraph [0011] and the block 202 shown in Figure 2 having the queue select line 222 which corresponds with the queue select line 122 in Figure 1 and the empty flags 224 which corresponds to receipt of the empty flags 114,116,118 shown in Figure 1. As to the arbitration table having multiple entries, this is clearly shown in Figure 2, where the arbitration table 202 has multiple entries 204,206,208,210,212,214,216, and 218. Support for this is specifically found in line 3 of paragraph [0011] in the application. As to the showing of the first multiplexer operatively receiving output from the first table entry and output from a second table entry in the arbitration table, this is clearly

shown in Figure 3. In Figure 3, the first table entry is labeled 308 and the second table entry is labeled 358. Multiplexer 312 will either receive the output of the first table entry 308 via line 310 or it will see the output of the second table entry via multiplexer 362, line 364 which is labeled the daisy-chain input. Support for this is found in paragraph [0014] of the present application, for example.

The Examiner rejects Claims 1-9 and 21 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The Examiner states that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Examiner states that regarding Claim 1, there is no adequate description on how the queues are related to the arbitrator. The Examiner states that the specification does not provide sufficient description of the logic circuit and specifically there is no clear and adequate description of the different inputs and outputs in Figure 3.

The rejection is respectfully traversed. As stated above, the present invention replaces the arbitration table shown in Figure 1 of the prior art with the arbitration table shown in Figures 2 and 3, for example. Thus, the way that the queues are related to the arbitrator is clearly shown in Figure 1 and a description thereof in paragraph [0005]. As to the description of Figure 3, this is clearly described in paragraph [0014] of the present application. The lines 318-322 and 368-372 are the three empty flag signals which come from the three queues as recited on the eleventh line of paragraph [0014]. The output of multiplexer 312 on line 314 is described in paragraph [0014] at lines 5-9. Specifically, line 314, if the first in the chain, is fed to the multiplexer such as multiplexer 124 shown as Figure 1, that selects the queue that's to send out data. Line 376 which is the input to multiplexer 362 is connected to the next slot in arbitration table 202. If that is the last slot in the table it is coupled to an arbitrary logic level. The TE output 310 from the first stage 302 is fed back to the equivalent of 374 of the highest number stage and shown by line 220 in Figure 2. That is, the output from the first stage 204 is connected to the input to the last stage 218. Lines 304 and

354 are the POP signal and lines 306 and 356 are the clock signal lines. The table entries are shown as 308 and 358, which correspond to two contagious table entries such as 204, 206 although any two contagious entries can be utilized.

The Examiner rejects Claims 1-9 and 21 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regard as the invention. The Examiner states that in regard to Claim 1, the arbitration table operation in conjunction the plurality of entries is not clear. It is not clear whether there is one logic circuit or many associated with entries.

This rejection is respectfully traversed. The arbitration table is recited as comprising a plurality of entries and the arbitration logic circuit is recited as comprising one circuit through each of the plurality of entries in the arbitration table. Therefore, it is clear that there is one arbitration logic circuit for each of the entries in the table.

The Examiner states that with regard to Claim 4, if no data is present in the data queue corresponding to the second table entry, data is selected from the next entry in the table which corresponds to the queue which has data to be sent out. The Examiner states that it is not clear what happens when there is no data to be sent out in the second table entry and any of the subsequent table entries.

This rejection is respectfully traversed. The purpose of the claims is not to explain how the invention works, that is recited in the specification. The purpose of the claims is to define the subject matter which Applicant claims as his invention. Applicant not claiming as the invention as described in Claim 4, how that problem is handled. It is not necessary for the claims to recite every possible problem that can come up in the operation of the circuit and claim that as the invention. Therefore, Applicants request that this rejection be withdrawn.

Applicants note that there is no rejections made for Claims 10-20, the statement on the Office Action Summary to the contrary notwithstanding. Therefore, Applicants understand these claims are allowed.

Accordingly, Applicants believe that the application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted by,
Texas Instruments Incorporated

/William B Kempler/
William B. Kempler
Senior Corporate Patent Counsel
Reg. No. 28,228
Tel.: (972) 917-5452